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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,801	02/18/2004	Makoto Ogawa	12377/6	9632
23838	7590	08/21/2007		
KENYON & KENYON LLP 1500 K STREET N.W. SUITE 700 WASHINGTON, DC 20005			EXAMINER FENNEMA, ROBERT E	
			ART UNIT	PAPER NUMBER
			2183	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/779,801	<b>Applicant(s)</b> OGAWA ET AL.	
	<b>Examiner</b> Robert E. Fennema	<b>Art Unit</b> 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 5/29/2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 11-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims 11-25 are pending. Claims 11-22 amended as per Applicant's request.  
Claims 23-25 added as per Applicant's request.

### ***Claim Objections***

2. Claim 11 is objected to for incomplete language. Claim 11, Line 3 reads: "...the inputted instruction code, and uniquely an instruction to be executed...". Examiner believes that the word "determines" should appear immediately after uniquely, in accordance with the other independent claims, and this is how Examiner has interpreted this line for the sake of examination, since the current language does not make sense. Correction or clarification is requested.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:  

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 15 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Both claims conclude with the phrase "when an instruction code, in which an instruction to be executed in accordance with the instruction code only is uniquely determined, is inputted". It is not very clear to the Examiner what is being claimed here, as the language is very confusing, and it is not clear what is going on when something is input. Examiner is interpreting this phrase in

both claims to indicate that an instruction is executed when an instruction code is input, however, Applicant is required to clarify or correct the language in the claim to make it more clear in the next response what subject matter is being claimed.

5. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 discloses that each instruction group has a group code, which is different from others in the instruction group. However, this does not make sense, because if each group has a group code, and there is no mention of any other group codes in the group, then what is it supposed to be different from if no others exist? Examiner is interpreting this limitation as saying that each group has a group code which is different than the group codes from other groups, however, Applicant is required to clarify or correct the claim such that it is clear what is actually trying to be claimed.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 11-18 is rejected under 35 U.S.C. 102(b) as being anticipated by Rotenberg et al. (herein Rotenberg).

7. As per Claim 11, Rotenberg teaches: An information processing unit,

comprising a decoder circuit selecting an instruction group corresponding to an inputted instruction code, based on a history of the inputted instruction code, and uniquely [determine] an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code (Section 2.2, based on the input instruction, a trace is selected from the trace cache and output to be executed), and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups (Section 2.2, second paragraph, the traces) and each instruction is given with an instruction code different from others within the same instruction group in advance (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), each instruction group having a certain instruction code to which an instruction belonging to another instruction group can be assigned (it is possible that an instruction with an address in one group will also appear in another trace, or be the target of the branch at the end of the trace, see Section 2.2, the branch fall-through and target addresses), and said decoder circuit outputting a control signal corresponding to the instruction assigned to the certain instruction code to a processor element, when said certain instruction code is inputted (Section 2.2, Second Column, Second Paragraph, upon a hit, the trace is fed to the instruction latch).

8. As per Claim 12, Rotenberg teaches: The information processing unit according to claim 11, wherein the instruction, which belongs to another instruction group and is

assigned to the certain instruction code, is changeable (Section 2.2, the traces can be modified).

9. As per Claim 13, Rotenberg teaches: The information processing unit according to claim 11, wherein each of the instruction groups has a plurality of the certain instruction codes to which an instruction belonging to the other instruction group can be assigned (See Claim 11 rejection, it is possible for the same addresses to show up in other traces, especially in the partial match and multiple path alternative embodiments described in section 2.3).

10. As per Claim 14, Rotenberg teaches: An information processing unit, comprising a decoder circuit retaining information corresponding to a history of inputted instruction codes, selecting an instruction group corresponding to an inputted instruction code based on the information, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code (Section 2.2, based on the input instruction, a trace is selected from the trace cache and output to be executed), and,

wherein said plurality of executable instructions are sorted into a plurality of instruction groups (Section 2.2, a trace) and each instruction is given with an instruction code different from other instruction codes within the same instruction group in advance (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), and said decoder circuit temporarily changes the information when a certain instruction

code is inputted (Section 2.2, traces can be modified or replaced depending upon the input, which necessarily results in changing the data).

11. As per Claim 15, Rotenberg teaches: The information processing unit according to claim 14, wherein said decoder circuit determines an instruction to be executed, based on the inputted instruction code only, irrespective of the information corresponding to the history of instruction codes, when an instruction code, in which an instruction to be executed in accordance with the instruction code only is uniquely determined, is inputted (Section 2.2, when there is a hit, the trace is fed to the instruction latch, starting with the instruction with the same address which was input).

12. As per Claim 16, Rotenberg teaches: An information processing unit executing an instruction determined in accordance with an inputted instruction, comprising a decoder circuit retaining information corresponding to an input history of a plurality of inputted instruction codes (Section 1.1), and uniquely determining an instruction to be executed, selected from a plurality of instructions which are assigned to the inputted instruction code in accordance with a combination of the information and the inputted instruction code (Section 2.2, based on the history of a trace and the incoming address, instructions are executed).

13. As per Claim 17, Rotenberg teaches: The information processing unit according to claim 16, wherein the decoder circuit determines an instruction to be executed

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selected from a plurality of executable instructions (Section 2.2), and the plurality of executable instructions are sorted into a plurality of instruction groups (Section 2.2, traces) and each instruction is given with an instruction code different from others within the same instruction group in advance (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1).

14. As per Claim 18, Rotenberg teaches: The information processing unit according to claim 16, wherein said decoder circuit determines an instruction to be executed, based on the inputted instruction code only, irrespective of the information corresponding to the history of instruction codes, when an instruction, in which an instruction to be executed in accordance with the instruction code only is uniquely determined, is inputted (Section 2.2, when there is a hit, the trace is fed to the instruction latch, starting with the instruction with the same address which was input).

### ***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg, in view of Patterson et al. (herein Patterson).

17. As per Claim 19, Rotenberg teaches: An information processing unit,
- a decoder circuit uniquely determining an instruction to be executed selected from a plurality of executable instructions based on an inputted instruction code and a group code corresponding to a history of the inputted instruction codes (Section 1.1, if a trace is encountered more than once, it is executed. The group code is the trace tag, see Section 2.2, Figure 4), and
- a processor element executing an operation corresponding to a control signal provided from said decoder circuit (Figure 1), and
- wherein said plurality of executable instructions are sorted into a plurality of instruction groups assigned by the group code (Section 2.2, the traces) and each instruction is given with an instruction code different from others within the same instruction group in advance (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), and the executable instruction includes an alias instruction to which an instruction belonging to the other instruction group can be assigned in advance to an internal instruction code constituted by the group code and the inputted instruction code (it is possible that an instruction with an address in one group will also appear in another trace, or be the target of the branch at the end of the trace, see Section 2.2, the branch fall-through and target addresses), but fails to explicitly teach:
- comprising a plurality of processors on one chip, each processor capable of executing instructions independently.

Rotenberg teaches a superscalar machine which can execute multiple instructions in one clock cycle, but does not teach having multiple processors in this system. However, Patterson teaches that the practice of using multiple processors is having a bigger role, due to being able to increase performance at a minimum of cost, and that the complexity of making processors more superscalar becomes a barrier (Pages 635-636). Given the advantage of increased performance for reduced cost, it would have been obvious to one of ordinary skill in the art to apply Rotenberg's invention to a machine with multiple processors, to further increase parallelism.

18. As per Claim 20, Rotenberg teaches: The information processing unit according to claim 19, wherein each of said processors further comprises a group register storing the group code, which is set up based on the history of the inputted instruction code (Section 2.2, Figure 4, the tag).

19. As per Claim 21, Rotenberg teaches: The information processing unit according to claim 20, wherein each of said processors further comprises a lookup table prescribing a change in a rule of the group code stored in said group register (Section 2.2 and Figure 4).

20. As per Claim 22, Rotenberg teaches: The information processing unit according to claim 21, wherein said lookup table is set up with a combination of an instruction

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mask for setting a mask bit, an instruction code for comparing the internal instruction code, and the changed group code (Section 2.2 and Figure 4).

21. As per Claim 23, Rotenberg teaches: The information processing unit according to claim 11, wherein each instruction group is given with a group code different from others in the instruction group in advance, and the group code corresponding to the inputted instruction code is determined based on the history of the inputted instruction code (Section 2.2, the tag, which is unique to each group).

22. As per Claim 24, Rotenberg teaches: The information processing unit according to claim 14, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group (Section 2.2, the tag, which is unique to each group).

23. As per Claim 25, Rotenberg teaches: The information processing unit according to claim 17, wherein the information corresponding to the history of inputted instruction codes is a group code for selected said instruction group (Section 2.2, the tag, which is unique to each group).

### ***Response to Arguments***

24. While Examiner appreciates the Applicant's attempt to explain the differences between the invention and the Rotenberg reference (and Patterson in the 103

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rejections), Examiner still feels that the claim language has not overcome the art.

Rotenberg does teach a plurality of instructions sorted into groups; the traces. Each instruction has a code which is different from the others in the trace (the address), and a plurality of instructions are assigned to one instruction code, as once the trace is accessed, all instructions can be used (See Section 2.2), thus multiple instructions are executed by only specifying one instruction (once the first instruction in the trace hits, the whole trace is executed). Instruction codes from one trace can be assigned to a different trace, depending upon the flow of the program (an instruction in the middle of one trace may be the beginning of another trace), and the data can be temporarily changed (depending on what is meant by temporarily, which is a fairly vague and non-descriptive term). These traces are also designed around a history of inputs, as the traces are constructed from instructions that are executing, in anticipation that they will execute again.

With this in mind, Examiner suggests trying to explain or claim in more detail the differences between the claimed invention and Rotenberg, because while it is possible that the claimed invention is not a trace cache, the current broad language of the claims fits in with what a trace cache is, and thus allows the trace cache to read upon the claims. Therefore, Examiner believes that putting a bit more detail into the claims may overcome the current rejections, and/or clarifying some of the limitations which were objected to, or rejected under 112, as some of the language in the claims is very confusing or indefinite, and it is possible that some of those limitations may help to overcome the art, once they can actually be understood.

***Conclusion***

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

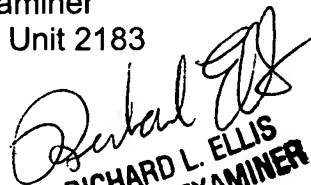
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema  
Examiner  
Art Unit 2183

RF

  
RICHARD L. ELLIS  
PRIMARY EXAMINER